IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A magnetic memory device, comprising

a plurality of bit lines and a plurality of word lines, intersecting one another without being in contact to make up a matrix;

a plurality of memory cells provided at intersections of said plurality of bit lines and said plurality of word lines, including at least one magnetic tunnel junction; a plurality of first switching means connected to first ends of said plurality of bit lines, being capable of switching the electrical connection between said first ends and a first power supply or a second power supply; and

a plurality of second switching means connected to second ends of said plurality of bit lines, being capable of switching the electrical connection between said second ends and said first power supply or said second power supply.

2. (Original) The magnetic memory device according to claim 1, wherein

said first switching means have first MOS transistors and second MOS transistors of the same conductivity type whose first main electrodes connected to said first ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively, and

said second switching means have third MOS transistors and fourth MOS transistors of the same conductivity type whose first main electrodes connected to said second ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively.

3. (Original) The magnetic memory device according to claim 1, wherein

said first switching means have first MOS transistors and second MOS transistors of different conductivity types whose first main electrodes connected to said first ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively, and

said second switching means have third MOS transistors and fourth MOS transistors of different conductivity types whose first main electrodes connected to said second ends of said plurality of bit lines, respectively, and second main electrodes connected to said first power supply and said second power supply, respectively.

4. (Original) The magnetic memory device according to claim 3, further comprising:

fifth MOS transistors connected between said first main electrodes of said first and second MOS transistors, having the same conductivity type as that of said second MOS transistors; and

sixth MOS transistors connected between said first main electrodes of said third and fourth MOS transistors, having the same conductivity type as that of said fourth MOS transistors,

wherein control electrodes of said fifth and sixth MOS transistors are connected to a third power supply supplying a predetermined voltage which always brings an ON state.

Claims 5 – 18 *(Cancelled)*